

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus for reducing a leakage current for a plurality of MOS transistors disposed in an integrated circuit, comprising:

a detection circuit for automatically generating an up signal and a down signal based on a determination as to what side of an inflection point that an initial value of the leakage current is disposed, wherein the inflection point is a graphical representation of a value for a back bias voltage that causes the least amount of leakage current from the plurality of MOS transistors, and wherein the detection circuit further includes at least two current mirrors that are arranged with complementary MOS transistors that have a relatively matched size; and

a bias circuit for automatically providing an adjusted back bias voltage that enables the least amount of leakage current by the plurality of MOS transistors, wherein if the up signal is generated, then the adjusted back bias voltage is increased and if the down signal is generated, then the adjusted back bias voltage is decreased, and wherein the biasing circuit provides a relatively constant value for the back bias voltage if both the up signal and the down signal are ungenerated by the detection circuit.

2. (Original) The apparatus of Claim 1, wherein the plurality of MOS transistors are PMOS transistors, wherein if the initial leakage current is disposed before the inflection point, the up signal is generated and the adjusted back bias voltage is increased, and wherein if the initial leakage current is disposed after the inflection point, the down signal is generated and the adjusted back bias voltage is decreased.

3. (Original) The apparatus of Claim 1, wherein the plurality of MOS transistors are NMOS transistors.

4. (Original) The apparatus of Claim 1, wherein the detection circuit further includes a logic circuit that activates the biasing circuit with up and down signals that are based on a comparison of at least three voltages generated by at least three leakage currents in at least two pairs

of MOS transistors of a relatively matched size, wherein the matched pairs of MOS transistors are coupled to separate current mirrors that are arranged with complementary MOS transistors that have a relatively matched size.

5. (Original) The apparatus of Claim 1, wherein the detection circuit further includes a logic circuit that employs at least three voltages to band the position of the inflection point, wherein the at least three voltages are generated by at least three leakage currents in at least two pairs of MOS transistors of a relatively matched size, wherein the matched pairs of MOS transistors are coupled to separate current mirrors that are arranged with complementary MOS transistors that have a relatively matched size.

6. (Original) The apparatus of Claim 1, wherein the detection circuit further includes at least two pairs of MOS transistors of a relatively matched size, wherein the matched pairs of the MOS transistors are sized substantially larger than a minimum size for the plurality of MOS transistors, and wherein the substantially larger size of the matched MOS transistors enables the initial leakage current to be detectable by the detection circuit.

7. (Cancelled)

8. (Original) The apparatus of Claim 1, wherein the back bias voltage is coupled to a substrate shared by the bulk terminals for the plurality of MOS transistors.

9. (Original) The apparatus of Claim 1, wherein the back bias voltage is a reverse bias voltage applied to a bulk terminal of the plurality of MOS transistors.

10. (Original) The apparatus of Claim 1, further comprising a battery that supplies power to the integrated circuit, wherein the reduction in the value of the leakage current causes a decrease in the amount of power drawn in an idle state by the integrated circuit from the battery.

11. (Currently Amended) An integrated circuit that reduces a leakage current for a plurality of PMOS transistors disposed in an integrated circuit, comprising:

a detection circuit for automatically determining on what side of an inflection point that an initial value of the leakage current is disposed, wherein the inflection point is graphical representation of a value for a back bias voltage that causes a least amount of leakage current from the plurality of PMOS transistors, wherein if the initial value of the leakage current is disposed before the inflection point, an up signal is generated, and wherein if the initial leakage current is disposed after the inflection point, a down signal is generated; and wherein the PMOS transistors in the detection circuit are of a relatively matched size that is substantially larger than a minimum size for the plurality of PMOS transistors, and wherein the substantially larger and matched size of the PMOS transistors in the detection circuit enables the initial leakage current to be detectable by the detection circuit; and

a bias circuit for automatically providing a back bias voltage that enables the least amount of leakage current by the plurality of PMOS transistors, wherein if an up signal is generated, then the magnitude of the back bias voltage is increased and if a down signal is generated, then the magnitude of the back bias voltage is decreased, and wherein the biasing circuit provides a relatively constant value for the back bias voltage if both the up signal and the down signal are ungenerated by the detection circuit.

12. (Original) The integrated circuit of Claim 11, wherein the integrated circuit is fabricated with a sub-micron process.

13. (Original) The integrated circuit of Claim 11, wherein the detection circuit further includes a logic circuit that activates the biasing circuit with up and down signals that are based on a comparison of at least three voltages that are adjusted to band the position of the inflection point, wherein the middle voltage is selected for the adjusted back bias voltage.

14. (Cancelled)

15. (Original) The integrated circuit of Claim 11, wherein the back bias voltage is a reverse bias voltage that is applied to a bulk terminal of the plurality of PMOS transistors.

16. (Currently Amended) An integrated circuit that reduces a leakage current for a plurality of NMOS transistors disposed in an integrated circuit, comprising:

a detection circuit for automatically determining on what side of an inflection point that an initial value of the leakage current is disposed, wherein the inflection point is graphical representation of a value for a back bias voltage that causes a least amount of leakage current from the plurality of NMOS transistors, wherein if the initial value of the leakage current is disposed before the inflection point, an up signal is generated, and wherein if the initial leakage current is disposed after the inflection point, a down signal is generated, and wherein the NMOS transistors in the detection circuit are of a relatively matched size that is substantially larger than a minimum size for the plurality of NMOS transistors, and wherein the substantially larger and matched size of the NMOS transistors in the detection circuit enables the initial leakage current to be detectable by the detection circuit; and

a bias circuit for automatically providing a back bias voltage that enables the least amount of leakage current by the plurality of NMOS transistors, wherein if an up signal is generated, then the magnitude of the back bias voltage is decreased and if a down signal is generated, then the magnitude of the back bias voltage is increased, and wherein the biasing circuit provides a relatively constant value for the back bias voltage if both the up signal and the down signal are ungenerated by the detection circuit.

17. (Cancelled)